Device Perspective for Black Phosphorus Field-Effect Transistors: Contact Resistance, Ambipolar Behavior, and Scaling

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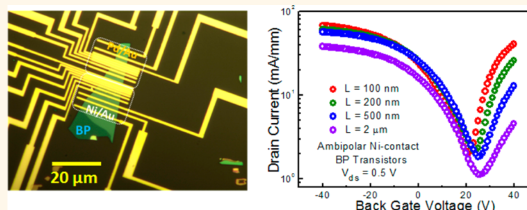
ABSTRACT Although monolayer black phosphorus (BP), or phosphorene, has been successfully exfoliated and its optical properties have been explored, most of the electrical performance of the devices is demonstrated on few-layer phosphorene and ultrathin BP films. In this paper, we study the channel length scaling of ultrathin BP field-effect transistors (FETs) and discuss a scheme for using various contact metals to change the transistor characteristics. Through studying transistor behaviors with various channel lengths, the contact resistance can be extracted with the transfer length method (TLM). With different contact metals, we find out that the metal/BP interface has different Schottky barrier heights, leading to a significant difference in contact resistance, which is quite different from previous studies of transition metal dichalcogenides (TMDs), such as MoS_2, where the Fermi level is strongly pinned near the conduction band edge at the metal/MoS_2 interface. The nature of BP transistors is Schottky barrier FETs, where the on and off states are controlled by tuning the Schottky barriers at the two contacts. We also observe the ambipolar characteristics of BP transistors with enhanced n-type drain current and demonstrate that the p-type carriers can be easily shifted to n-type or *vice versa* by controlling the gate bias and drain bias, showing the potential to realize BP CMOS logic circuits.



KEYWORDS: black phosphorus · phosphorene · Schottky barrier transistor · contact resistance · short-channel effect

Low-dimensional materials are garnering more and more interest in condensed-matter physics, materials, and device communities. They provide a new class of materials that are atomic-layer thick. Graphene, boron nitride, and transition metal dichalcogenides (TMDs) provide the ideal metal, insulator, and semiconductors as three basic building blocks for any device applications.[1−15] Transistors built on monolayer or few-layer MoS_2, the most studied TMDs, are the optimal forms of ultra-thin-body field-effect transistors (FETs) with an ideal structure to protect against the short-channel effects.[9,13] Also, the comparatively heavier effective mass of the MoS_2 allows transistors to have lower direct source−drain leakage current, increased drive current, and enhanced transconductance when benchmarked against the ultra-thin-body Si transistors at their scaling limit.[14] However, the carrier mobility of MoS_2 is much lower than that of graphene or traditional semiconductors.[16] Due to the presence of S vacancies and strong Fermi-level pinning near the conduction band,[17] MoS_2 transistors monotonically show n-type FET characteristics even when using high-work-function contact metals.[18]

The quest for p-type 2D materials is needed to build energy-efficient 2D electronic or optoelectronic devices such as CMOS, tunneling FETs, photodetectors, and solar cells beyond 2D Schottky barrier FETs. In this paper, we take a deep look into the metal/BP interface from the device aspects by applying different high-work-function metals (Ni and Pd) on BP field-effect transistors with channel lengths scaling from 3 μm down to 100 nm. Black phosphorus (BP), the bulk counterpart of phosphorene, is a stable phosphorus allotrope at room temperature.[19,20] BP has a layered structure in which individual atomic layers are stacked together by van der Waals interactions.[21−23] The fundamental properties of

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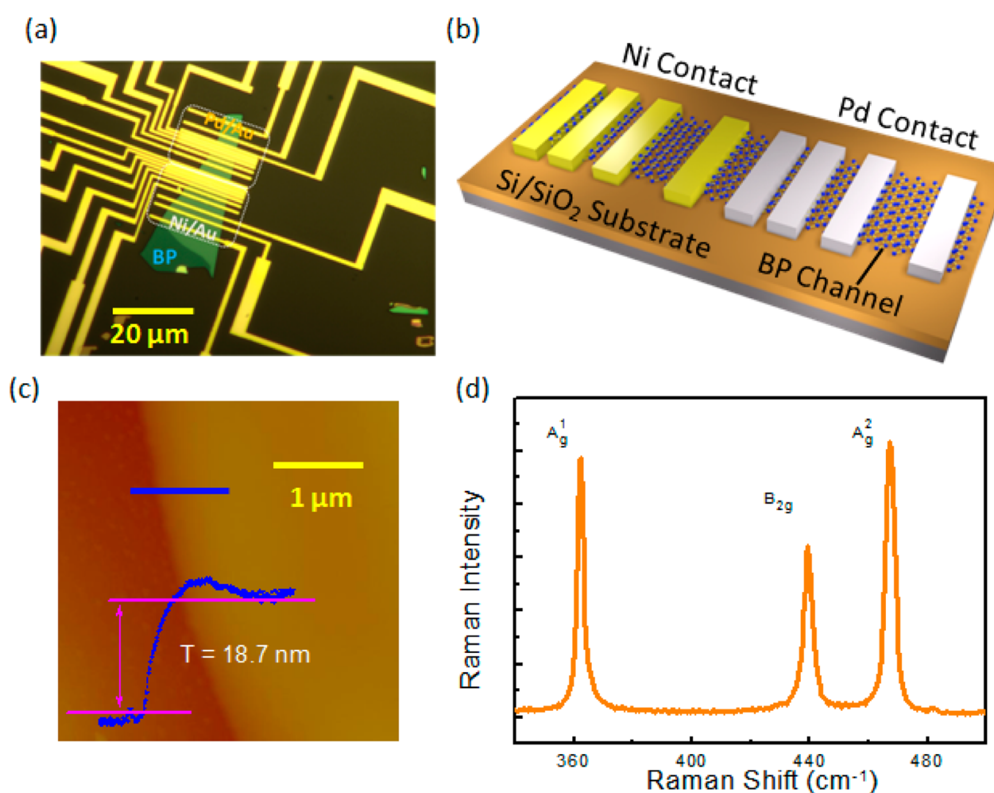

Figure 1. (a) Optical image of ultrathin BP FETs with Ni/Au and Pd/Au contacts on the same BP flake. (b) Schematic view of device configuration. A p^{++} silicon wafer capped with 90 nm of SiO_2 was used as the global gate and gate dielectric, respectively. Ultrathin BP films were exfoliated from bulk BP crystals. Metal contacts with various channel lengths from 3 μm down to 100 nm for both Ni/Au and Pd/Au were evaporated onto the same BP flake. (c) Atomic force microscopy image of this large size BP film with a measured thickness of 18.7 nm. (d) Raman spectra of the same BP film.

bulk BP had been extensively studied in the past, indicating the bulk crystal of BP is a semiconducting material with a direct band gap of 0.3 eV,[19,21,23] and the hole mobility in black phosphorus can reach up to 10^4 $cm^2/(V\ s)$.[24] The new wave of interest in BP is inspired by graphene research, an attempt to realize monolayers of BP, coined as phosphorene. Although phosphorene has been successfully exfoliated and its optical properties have been explored,[25] most of the electrical performance of the devices is demonstrated on few-layer phosphorene and ultrathin BP films.[25−29] This is because phosphorene is less stable in air, in particular in the presence of both oxygen and water.[30] An effective passivation technique on phosphorene is needed for practical applications. Here, we focus on ultrathin BP films since the large size of the flakes (tens of μm) is needed so that we can fabricate numerous FETs with two different metals on the same flake for a fair comparison, as shown in Figure 1a. Fortunately, few-layer or ultrathin 2D films are more favorable for device demonstrations because they can deliver a larger current than a monolayer in general. We determine a contact resistance of Ni and Pd on BP of 1.75 $\pm$ 0.06 $\Omega\cdot$mm *versus* 3.15 $\pm$ 0.15 $\Omega\cdot$mm at a high electrostatic doping limit. Furthermore, the characteristics of BP transistors with Ni contacts can be switched from a p-type behavior to pronounced n-type once scaled down to deep submicrometer channel lengths. The results all confirm the nature of Schottky barrier FETs for BP transistors with their smaller band gap.

RESULTS AND DISCUSSION

In our experiments, a large BP flake of ~40 μm × ~20 μm was exfoliated from bulk BP crystal using the Scotch tape method and then transferred to a heavily doped silicon substrate with a 90 nm SiO_2 capping layer. Prior to device fabrication, the ultrathin BP film was soaked in acetone for 2 h to remove tape residues. Contact bars with lengths of 0.5 μm were defined by e-beam lithography. The channel lengths are designed to be 3 μm, 2 μm, 1.5 μm, 1 μm, 500 nm, 200 nm, and 100 nm. Both 30/50 nm Ni/Au and 30/70 nm Pd/Au, deposited via e-beam evaporation, were used as contact metals on the same BP flake for a fair comparison. The optical image and schematic view of the ultrathin BP FETs are illustrated in Figure 1a and b, respectively. The thickness of BP for this study is 18.7 nm, as shown in Figure 1c, measured by atomic force microscopy (AFM). The Raman spectrum of the channel area of the BP FET is depicted in Figure 1d. The peaks at 362, 439, and 467 cm^{-1} are due to vibrations of the crystalline lattice of the BP, and they match the Raman shifts attributed to the A^1_g, B^2_g, and A^2_g phonon modes

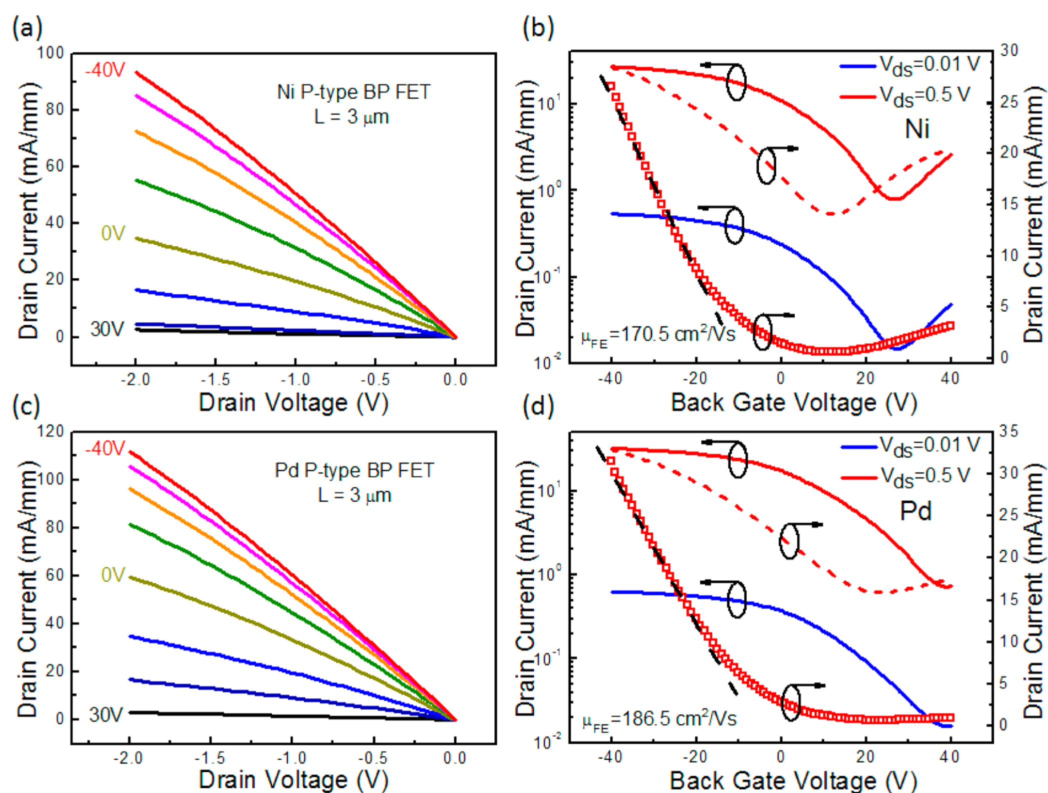

Figure 2. Device performance of p-type BP transistors for both Ni and Pd contacts. Output (a) and transfer (b) characteristics of a Ni contact BP transistor with a channel length of 3 μm. Output (c) and transfer (d) characteristics of a Pd contact BP transistor with a channel length of 3 μm. The arrow directions in the transfer curves stand for back gate sweep directions. Gate bias sweeps from −40 to 40 V for Ni and Pd transfer characteristics are shown in both semilogarithmic scale (red dashed lines) and linear scale (red squares).

observed in bulk black phosphorus and recent Raman studies of phosphorene.[25,27,28]

I−*V* output characteristics of an 18.7 nm thick, 3 μm long, BP FET with Ni contact are shown in Figure 2a with a back gate sweep from −30 to 40 V. On-state current increases as the back gate sweeps from positive voltage to negative voltage, which is a clear signature of p-type transistor behavior. The drain current varies linearly with small source/drain biases, demonstrating an ohmic-like contact resistance at the metal/BP interface with a small Schottky barrier. An on-state drain current of 93.3 mA/mm for the 3 μm channel length in the Ni contact device is observed with $V_{bg} = -40$ V and $V_{ds} = -2$ V. The transfer curve of the Ni device measured at 0.01 and 0.5 V drain bias is shown in Figure 2b. The transistor shows a clear switching behavior with a low current on/off ratio of $\sim 10^2$, due to the thick flake and low band gap of BP.[25−27] Inspecting the transfer behavior of the p-type BP transistor, we can estimate the field-effect mobility by referring to the simple square-law theory. The extrinsic field-effect mobility, μ_{FE}, is 170.5 cm^2/(V s), as calculated from $\mu_{FE} = g_m L/(C_{ox} V_{ds} W)$, where C_{ox} is the capacitance of the gate oxide, W and L are the channel width and length, V_{ds} is the drain bias, and g_m is the peak transconductance extracted from the linear scale of transfer behaviors. The hysteresis from different back gate sweeps is due to the fixed charges in thick SiO_2, the interface traps between the BP and the SiO_2 substrate, and charge transfer from/to neighboring adsorbates on the BP surface. This is commonly observed on 2D devices with an exposed surface in the ambient.[31] The *I*−*V* characteristics of the Pd contact device, as shown in Figure 2c and d, demonstrate inspiring electronic behaviors. Compared to the Ni contact device, the Pd transistor exhibits superior performance in on-state current and mobility. Examining the device with the same geometry as above, the Pd contact device has a drain current of 111.8 mA/mm and extrinsic field-effect mobility of 186.5 cm^2/(V s). This larger on-state current of the Pd transistor suggests that the Pd/BP contact has a smaller contact resistance compared to the Ni/BP contact. Note that similar threshold voltages (V_T) are observed for both devices, where the V_T-induced deviation can be fairly ignored in the contact resistance comparison. However, if we take a close look at the off-state current at large positive back gate voltage from transfer curves, there is an obvious difference depending on the contact metals. For Ni BP transistors, as the back gate bias sweeps from +26 V to +40 V in Figure 2b, we clearly observe an increase in the drain current, indicating an n-type transistor behavior. As it shows both strong n-type and p-type behaviors in the drain current, it is

classified as an ambipolar transistor, which is rarely seen in previous MoS_2 transistor studies. However, it is barely seen in high-work-function Pd contact BP transistors, which show only a monotonic enhancement of p-type drain current with decreasing gate voltage from $+40$ V to -40 V. Note that the results presented here are also consistent with a previous publication.[25] Due to ultrathin channel thickness and improved electrostatic control, long-channel few-layer phosphorene FETs have a high current on/off ratio and negligible ambipolar behavior even with Ti or Ni contacts.[25] A detailed examination of the Schottky barrier effects on two contacts of BP, which will be discussed in the later parts of this paper, helps us determine the switching mechanism of BP FETs for both p-type and n-type characteristics.

The contact resistance for both Ni and Pd contacts are extracted from the transfer length method (TLM) structure within the long-channel regime. Similar to the MoS_2 transistors, the contact resistance of BP transistors shows a strong gate-dependent behavior as well. The decrease of R_c at lower gate bias is related to the increase of electrostatically doped carrier density in BP under the metal contacts. The higher carrier density induced by the negative back gate voltage enhances the carrier concentration in the BP flake, which leads to a narrower Schottky barrier. Meanwhile, the narrowed Schottky barrier would thus facilitate the hole injection from the metal into the valence band of BP, leading to a lower contact resistance.[18] To exclude the large absolute errors, high negative bias regions are appropriate for a direct comparison of the contact resistance. As measured using TLM structures, the Pd contact resistance is $1.75 \pm 0.06\ \Omega \cdot$mm at $V_{bg} = -40$ V, which is much smaller than the Ni contact resistance of $3.15 \pm 0.15\ \Omega \cdot$mm at the same back gate voltage. This nearly 1.8 times reduction in contact resistance is mainly attributed to the different work function of the contact metals. The higher work-function metal Pd, with 5.4 eV, shows a significantly smaller contact resistance than the 5.0 eV metal Ni. Previous MoS_2 contact studies had demonstrated that the contact metals were heavily pinned near the conduction band of MoS_2 due to its S vacancies at the interface, where both low-work-function and high-work-function metals had similar contact resistances.[18,32] The transfer lengths (L_T) of BP transistors are extracted by the TLM curve[33] and are determined to be 0.72 μm for Pd contact and 1.18 μm for Ni contact at the on-state for a 10–20 nm BP channel. We should note that the contact width in our experiment is designed as 0.5 μm to maximize the number of contact bars on the same BP flake. The designed contact width is a little bit smaller than the calculated transfer length for both metals, indicating a nonfull carrier injection from the metals into the semiconductor material.[34] This suggests that the extracted contact resistances for both Ni and Pd are overestimated, where the actual contact resistance should be even smaller as the contact width could be made larger than the transfer length. By examining the channel length scaling, we observed clear ambipolar characteristics for both Ni- and Pd-contacted BP FETs at shorter channel lengths. As depicted in Figure 3b and c, enhanced electron current for BP transistors exhibit a strong channel-length-dependent behavior, where the short-channel device with a 100 nm channel length demonstrates a better n-type performance compared to the long channel length of 2 μm. A detailed explanation for channel-length-dependent ambipolar behavior will be provided later in this paper. Notably, contact metals causing an n-type performance difference between Ni and Pd is also elucidated in short-channel devices. Ambipolar behavior becomes much more pronounced if low-work-function-metal Ni is used for BP FETs. The reason for the more pronounced ambipolar behavior in Ni contact BP FETs is directly attribute to no strong Fermi-level pinning at the metal/BP interface, where the Ni metal Fermi level is closer to the conduction band, resulting in a smaller effective Schottky barrier height compared to high-work-function-metal Pd. In our experiments, a total of four sets of TLM structures, where each set is on the same BF flake, were carefully fabricated and systematically measured. The results obtained support the conclusion of minimal Fermi-level pinning at the metal/BP interface.

From the classical square-law theory, the drain current is inversely proportional to the channel length L_{ch}, where the drain current I_d should be presented as a linear behavior with $1/L_{ch}$. Shown in Figure 4a, the drain current extracted at $V_{ds} = 0.5$ V and $V_{bg} = -40$ V exhibits a linear relationship at long-channel regions. However, starting from a 500 nm L_{ch}, the drain currents begin to deviate from the inversely proportional behavior. The Pd contact current starts to saturate at 105.9 mA/mm at $L_{ch} = 100$ nm, and the Ni contact at 67.7 mA/mm as well. Similar to MoS_2 transistors, as we scale the BP FET channel length down to 500 nm, the contact resistance starts to be dominant in total resistance. The drain voltage applied on the BP FET mainly drops at the two contacts, where the contact resistance does not scale with channel length but is present in the device when the contact resistance is comparable to sheet resistance.[18] Next, intrinsic field-effect mobility *versus* channel length was studied in BP transistors. The intrinsic carrier mobility, μ_{FE}', is estimated by $\mu_{FE}' = \mu_{FE}(1 - 2g_m R_c)^{-1}$. As plotted in Figure 4b, Ni and Pd are presenting similar intrinsic field-effect mobility, indicating a good uniformity of our ultrathin BP flake, on which both Ni and Pd contacts are fabricated. Moreover, a decrease of mobility as the device channel length shrinks down to 100 nm is realized. This decrement is widely observed at any short-channel devices due to the fact that carriers are approaching their

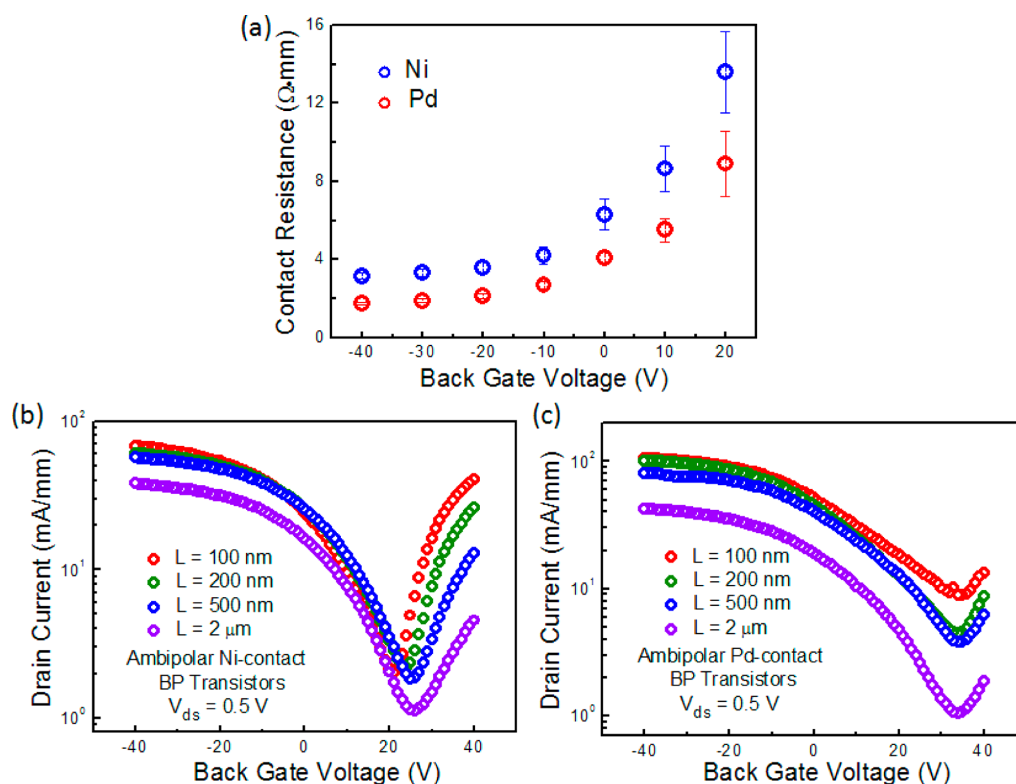

Figure 3. (a) Contact resistance for both Ni and Pd contact metals at various gate biases. Error bars are determined from the standard errors of the linear fitting under different back gate biases. (b) *I*−*V* transfer characteristic of Ni contact BP FETs with a channel length from 2 μm to 100 nm. (c) *I*−*V* transfer characteristic of Pd contact BP FETs with a channel length from 2 μm to 100 nm.

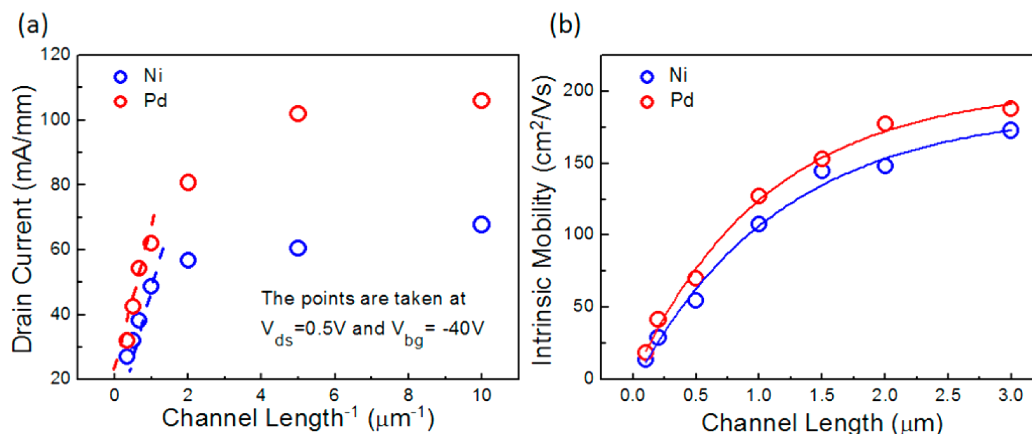

Figure 4. (a) On-state drain current measured at −40 V back gate bias and 0.5 V drain bias on the set of devices fabricated with various channel lengths. The linear dependence property in the diffusive region is indicated by the dashed line. (b) Channel-length-dependent intrinsic field-effect mobility from the set of BP transistors. Ni fitting curve coincides with the Pd fitting curve showing mobility is the fundamental property of the BP film itself after extracting contact resistances.

saturation velocities at the higher electrical fields.[7,18] The general $v-E$ relationship represents $v = \mu E$, and the electrical field in the channel is inversely proportional to channel length. At the low electrical fields, the mobility is constant. However, in the short-channel case of very high electrical fields, the velocity starts to approach a value, that is, saturation velocity, v_s, due to the scattering effect and ballistic transport. Therefore, as the velocity reached the saturation value, any further increment of the electrical field by scaling the channel length down would result in a decrement of calculated field-effect mobility.[18,34]

Knowing the nature of the Schottky barrier in BP transistors is essential to understand the transistor characteristics. In the previous paragraph, we discussed how the gate bias changes the effective barrier height at the different contacts and hence controls the carrier injection at the metal/BP interface. In this part, we further discuss how the drain bias modulates the two Schottky barriers at the contacts and also the

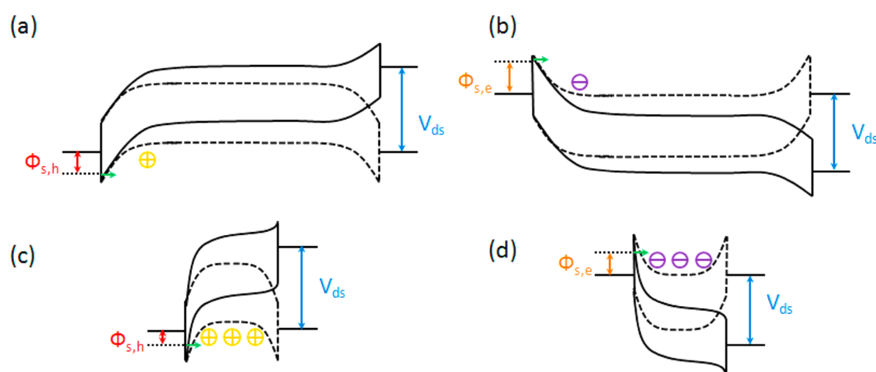

Figure 5. (a) Band diagram for a long-channel-length BP transistor with p-type behavior. The dashed line stands for $V_{ds} = 0$ V, and the solid line stands for $V_{ds} \leq 0$ V. (b) Band diagram for a long-channel-length BP transistors with n-type behavior. The dashed line stands for $V_{ds} = 0$ V, and the solid line stands for $V_{ds} \geq 0$ V. (c) Band diagram for a short-channel-length BP transistor with p-type behavior. The dashed line stands for $V_{ds} = 0$ V, and the solid line stands for $V_{ds} \leq 0$ V. (d) Band diagram for a short-channel-length BP transistor with n-type behavior. The dashed line stands for $V_{ds} = 0$ V, and the solid line stands for $V_{ds} \geq 0$ V.

switching mechanism of the BP transistors.[34] Similar to MoS_2 transistors, there are two asymmetrical Schottky barriers formed at the metal contacts of BP transistors, named as drain barrier and source barrier. However, compared to MoS_2 transistors, where the drain bias and gate bias can control only the on and off states due to its large band gap, bias modulations in BP transistors are even more complicated and interesting. Not only can the on and off states be modulated, transistor polarization and n-type and p-type transport behaviors can also been controlled by the drain bias and gate bias. Due to BP's small band gap, the original p-type behavior of BP transistors can be easily turned into n-type transport by controlling the channel length, back gate voltages, and drain biases. This kind of transistor characteristics is not easily observed in MoS_2 due to its large band gap and strong contact Fermi-level pinning near the conduction band edge.[35]

We first define the carrier path for both p-type and n-type BP transistors from the source to drain, in which the holes and electrons would encounter the source barrier first, where the carriers would undergo a thermal-assisted tunneling process from the source metal Fermi level to the channel. On the other hand, the carriers in the channel go from the valence band or conduction band back to the drain metals, for p-type or n-type, respectively. Let us first look at the intrinsic p-type BP transistors with a long channel length, as depicted in Figure 5a. Under large negative gate biases, source and drain contacts start to form the two triangle-shaped Schottky barriers. With a further increase of the drain bias, the barrier at the source end remains constant; meanwhile, the drain barrier vanishes, facilitating carrier movement from the source to the drain.[34] To investigate the mechanism of characteristics switch from p-type behavior to n-type, we perform a large positive gate bias for long-channel BP transistors, shown in Figure 5b. Due to the nature of the small-band-gap structure, carriers can overcome the Schottky barrier at the source and move along in the conduction band, showing ambipolar behavior with a moderate n-type drain current. With an adequate understanding of long-channel BP transistors, the bias-induced switching mechanism on short-channel devices remains to be elucidated. When the channel length is aggressively scaled down, the drain is close to the source, and the drain bias can start to affect the source barrier, such that the channel carrier concentration is no longer fixed. For long-channel devices, a drain bias can change the effective channel length, but the barrier at the source end is independent of the drain bias. However, for a short-channel device, the source barrier is no longer fixed. An increase of the drain bias causes the lowering of the source barrier, leading to the injection of extra carriers into the channel,[36] as shown in Figure 5c. It is similar to drain-induced barrier lowering (DIBL) in short-channel Si MOSFETs, where the drain bias decreases the source barrier, thus enhancing the off-state current, and makes the device more difficult to turn off.[36] Nevertheless, we need to carefully identify the short-channel effects related to BP transistors. In our previous publication, we proposed the drain-induced barrier narrowing (DIBN) model for MoS_2 transistors, where the narrowed barrier would reduce the Schottky barrier width at the source side and enhance the on-state current.[34] Here, we would like to describe the effect as the drain-induced characteristic switch (DICS) in BP field-effect transistors. As shown in Figure 5d, BP transistors with a short channel length under positive back gate bias and drain bias can easily experience unexpected electron movement along the conduction band, where the device demonstrates pronounced ambipolar behavior. Our experimental observations perfectly matched the proposed DICS effects, which are shown in previous results of Figure 3b and c. The scaling of the channel length down to 100 nm helps the drain bias start to have an impact on the source

ends. The lowering of the source barrier would facilitate greater electron injection into the conduction band, and the devices would exhibit stronger ambipolar behavior with enhanced n-type drain currents. The DICS effect on BP transistors will become more obvious as the channel length aggressively scales down to the sub-100 nm regime. The geometrical screening length with a planar structure is $\lambda = ((\varepsilon_s/\varepsilon_{ox})t_s t_{ox})^{1/2}$, where λ is the geometrical screening length, $\varepsilon_s = 10$ is the permittivity of BP,[28,37] ε_{ox} is the permittivity of the gate oxide, and t_s and t_{ox} are the thickness of the semiconductor channel and gate oxide. The geometrical screening length for this 18.7 nm BP flake is 65.7 nm, which is comparable to or only a little shorter than our shortest channel length device. In the extreme case where the channel length approaches the screening length, the n-type drain current becomes a strong function of the drain bias, where the n-type behavior may be dominant in BP ambipolar characteristics with a low-work-function metal, such as Y, La, or Sc. Even with Al metal contacts, our preliminary experimental result shows a pronounced ambipolar effect at larger channel lengths. Our observations in ambipolar BP transistors open a new way to adjust transistors' polarity from p-type to n-type along with the development of doping techniques in 2D materials[38] and possible realization of 2D CMOS circuits based on the same channel material, BP.

CONCLUSION

In summary, we have studied the BP transistors' behaviors with two different high-work-function contact metals. The 0.6 eV work-function difference between Ni and Pd leads to a significantly lower contact resistance on BP using Pd. We explained the switching mechanism of BP transistors, which are controlled by two Schottky barriers at the metal contacts. Moreover, the device characteristics can be alternated from intrinsic p-type to n-type behavior by proper modulation of the channel length, gate bias, and drain bias. With the further development of doping technique and contact engineering, BP transistors show the potential for 2D CMOS logic circuits.

METHODS

Multilayer BP was exfoliated from the bulk crystal black phosphorus (Smart-elements) and then transferred to a 90 nm SiO_2 substrate. All samples were sequentially cleaned by acetone, methanol, and 2-propanol to remove the Scotch tape residues and then stored in a nitrogen atmosphere. The thickness of the BP was measured using a Veeco Dimension 3100 atomic force microscope. The Raman optical measurement was conducted in a microscope coupled to a grating spectrometer with a CCD camera. E-beam lithography was used to define the source and drain patterns, using a Vistec VB6; 30/50 nm Ni/Au and 30/70 nm Pd/Au were deposited using e-beam evaporation under 10^{-6} Pa pressure, with a deposition rate of 1 Å/s. No annealing was performed after the deposition of the metal contacts. Electrical measurements were carried out with a Keithley 4200 semiconductor parameter analyzer and probe station in ambient atmosphere.

Conflict of Interest: The authors declare no competing financial interest.

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